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Performance analysis and simulation of vertical gallium nitride nanowire transistors

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ABSTRACT

Gallium nitride (GaN) nanowire transistors are analyzed using hydrodynamic simulation. Both p-body and n-body devices are compared in terms of threshold voltage, saturation behavior and transconductance. The calculations are calibrated using experimental data. The threshold voltage can be tuned from enhancement to depletion mode with wire doping. Surface states cause a shift of threshold voltage and saturation current. The saturation current depends on the gate design, with a composite gate acting as field plate in the p-body device.

1. Introduction

Gallium nitride (GaN) based transistors have shown excellent performance in terms of breakdown voltage, switching speed, and on-resistance [1]. Compared to Silicon transistors, GaN planar transistors still face challenges concerning enhancement mode (E-mode) operation and dynamic current collapse. Vertical transistor architectures can potentially solve these challenges, by placing the gate metal on a non-polar sidewall [2,3]. For fin-structures, excellent results have been reported, with blocking voltages of 800 V at 0 V bias, and low on-resistances [2]. Another vertical approach is the use of nano- or microwires, which use a wrap-around gate for optimum electrostatic control [4,3]. Besides of that, vertical wire transistors can be free of strain issues when grown on foreign substrates, and efficiently scale down the active device area, which is promising for both logic and switching applications [5]. Particularly, GaN nanowire based direct coupled FET logic, using both E- and D- mode nanowire FETs, can be used as a smart driving circuitry for monolithic integration with other functionalities (e.g., GaN LEDs, HEMTs) in principle [6]. Simulation of the high voltage characteristics has been demonstrated [7].

In this paper, nanowire transistor experiments are analyzed using a hydrodynamic simulation method. The experimental structures are enhancement mode (E-mode) and depletion mode (D-mode) transistors arranged as an array, with bottom source and top drain contacts. The wrap around gate is placed on an SiO_2 dielectric layer. Devices with electron channels in an n-doped region (n-body) and in a p-doped region (p-body) have been realized. Threshold voltages, current saturation and transconductance are calculated and compared to experiment, and the impact of surface states is discussed.

2. Device structure

We compare three different nanowire designs, which vary in wire doping, radius and layer thicknesses. All designs have been implemented and characterized experimentally as transistor arrays [4,8]. Fig. 1 shows the cross-section of a single nanowire, and Table 1 contains the dimensions, as taken from experiment. The gate length is denoted by L, and the gate width is the circumference of the wire. In the left figure a, the channel region is formed by low-doped n-type GaN, resulting in an n-body enhancement mode transistor. The center device b is a depletion mode transistor, where the n-body has higher doping, which prevents the wire from being depleted in the off state. The right device c consists of a stack of npn layers, and is an E-mode transistor. In all devices, the electron drift layer is part of the n_2 layer between the gate and the highly doped n_1 layer. The Cr gate metallization is placed on a SiO_2 layer with 20 nm thickness. Details of the device fabrication can be found in [4].

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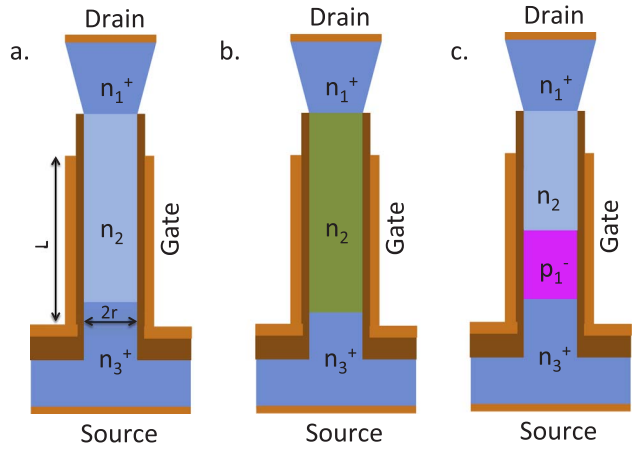

Fig. 1. Device structures of nanowire transistor. (a) n-body E-mode (nin-device), (b) n-body D-mode (nnn-device), (c) p-body E-mode (npn-device). The passivation layer (dark brown) consists of SiO_2, and a Cr layer for metallization (light brown). (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

Table 1
Structural data of nanowire transistors. The oxide thicknesses of 20 nm and 220 nm are set on the wire sidewall (gate) and the substrate, espectively.

	r (nm)	L (μm)	Doping ($1e18cm^{-3}$) $n_1^+/n_2/n_3^+/(p_1^-)$	Thickness (μm) $n_1^+/n_2/n_3^+/(p_1^-)$
nin	180	1.7	10/0.02/1	0.5/2.0/0.2
nnn	115	1.6	10/1/1	0.5/2.0/0.2
npn	235	1.8	10/0.3/3/(1)	0.5/1.6/0.2/(0.5)

3. Simulation model and material parameters

In order to model carrier transport in the presence of high electric fields, a hydrodynamic simulation is employed. We use the Synopsys SDevice software [9] and the wire is represented by a two-dimensional cross section with rotational symmetry. The experimental device has a hexagonal footprint, which is approximated by a cylindrical simulation geometry. Energy flux equations are solved only for electrons, for holes the standard drift–diffusion system is applied. This is necessary to account for velocity overshoot effects, especially in the drift region of the transistor, where the electrons do not follow an equilibrium Fermi–Dirac distribution [10].

Shockley–Read–Hall (SRH) and Auger recombination add recombination terms to the system, with parameters taken from [11]. The low-field carrier mobility is a Masetti model, which includes a dopant density dependence [12]. The high field characteristics are represented by a Canali model which is based on the Caughey-Thomas formula [13]. The main parameters of the mobility model are given in Table 2. The band structure parameters for GaN have been taken from [14]. Incomplete ionization of Mg acceptors in GaN has been modeled with a Shockley model and an activation energy of $E_a = 180$ meV [15]. Quantization effects are not considered in the simulation.

The simulation results in a self-consistent solution of Poisson equation, carrier continuity equation for electrons and holes, and energy flux equations for electrons.

Table 2
Simulation parameters for the mobility model.

E_g(300 K)	3.4 eV
$\mu_{low,e}$	1200 cm^2/Vs
$\mu_{low,h}$	20 cm^2/Vs
$v_{sat,e}$	2.2×10^7 cm/s

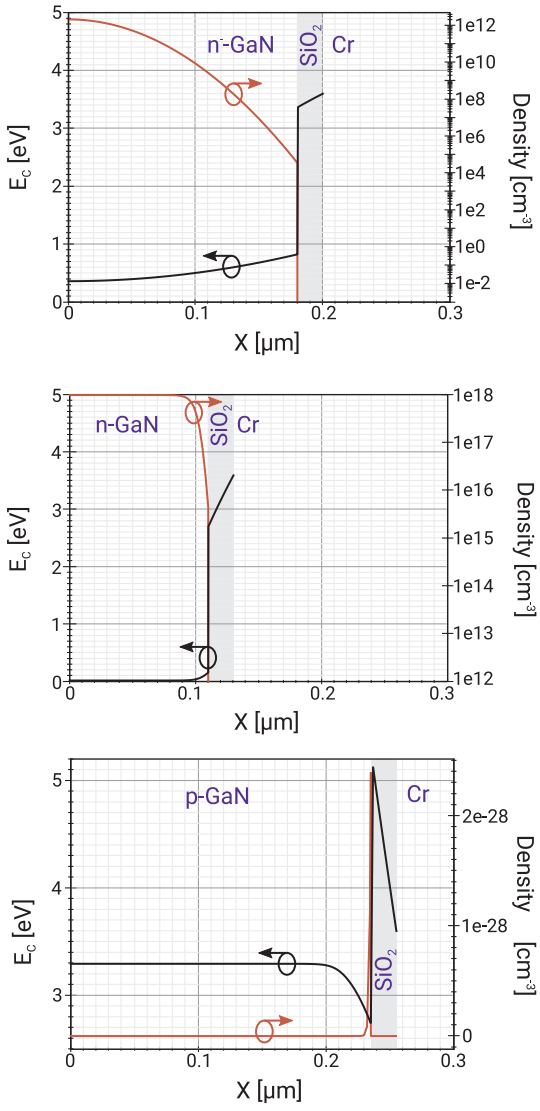

Fig. 2. Conduction band and electron density (red) in radial direction at $V_{DS} = V_{GS} = 0$ V. Top: n-channel E-mode, center: n-channel D-mode, bottom: p-channel E-mode. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

4. Threshold analysis

The gate characteristics can be understood from the metal–insulator-semiconductor (MIS) interface physics. In our case, the band alignment at the Cr-SiO_2-GaN interface is determined by the work-function of Cr (4.5 eV) [16] and the electron affinity in unpolar GaN (3.4 eV), as well as the charges from the wire doping, and potentially any interface charges. Fig. 2 shows the conduction band and electron density for a radial cut from the wire center to the surface at $V_{DS} = V_{GS} = 0$ V in the gate region. For the case of the low $N_d = 2 \times 10^{16}$ cm^{-3} doped nin-device (top figure), the work function of the metal is larger than in the semiconductor. The wire is fully depleted at $V_{GS} = 0$ V, leading to normally-off characteristics. The threshold voltage results from the gate potential required to compensate for the wire depletion, which is according to the TCAD simulation $V_{th} = 0.8$ V. This is close to the experimental value of 1.2 V [4]. The difference can be explained by negatively charged surface states as observed in [17] for m-plane surface GaN nanowires. In the simulation, additional surface charges at the wire surface of $n_s = 6 \times 10^{11}$ cm^{-2} lead to a threshold